Modeling GaN: Powerful but Challenging

GaN

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Gallium nitride transistor-based power amplifiers (PAs) are currently among the most important technologies impacting high-power transmitter design at microwave frequencies. The high breakdown voltage capability (over 100 V), combined with simultaneous high-current capability (tens of amps) and favorable thermal conductivity of modern aluminum gallium nitride/gallium nitride high-electron mobility transistors (AlGaN/GaN HEMTs) (often more simply referred to as GaN HEMTs) on silicon carbide (SiC) and silicon substrates, has enabled an order-of-magnitude improvement in power density over gallium arsenide (GaAs)-based devices. GaN HEMTs also allow high-power operation at much higher frequencies than silicon laterally diffused metal–oxide–semiconductor field-effect transistors (LDMOS FETs), currently a staple for the cellular base station industry. As GaN technology has developed, first in research laboratories and more recently in multiple commercial device manufacturers, the demand for improved nonlinear models has grown alongside the device process improvements. The need for improved models for GaN is twofold: first, GaN devices have unique nuances in behavior to be addressed; second, there is a desire for improved accuracy to take full advantage of the performance wins to be gained by GaN HEMT performance in the areas of high efficiency and high-power operation.

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Such behavioral nuances include trapping effects and associated current-knee collapse (which results in an increase in the knee voltage at which electron velocity saturation occurs) that tends to be more significant for GaN than for GaAs-based HEMTs, as illustrated by Trassaert et al. [1] and Charbonninud et al. [2]. Additional bias dependences have been observed, for example, in the source resistance, as pointed out by Trew et al. [3], and the drain-to-source capacitance, as indicated by Tajima [4]. Subthreshold-valid modeling may be important for designers who wish to operate in Class B, C, D, and E high-efficiency operating modes, for example, and not all models can fit behavior in this region. Specific attention was paid to ensure the Curtice FET (CFET) model [5] is well behaved in this region. Candidate models should be checked for fidelity with respect to measured data for gate voltages at or below threshold if this operating region will be important for the application. Finally, due in part to the capability of GaN HEMTs to work at higher voltage-current products, there is an increased need for accurate electrothermal modeling. Illustrative work in this area can be found in the works of Camarchia et al. [6] and Casto [7], among many others [2], [7]–[9].

The significant attention placed on nonlinear models is in step with the growing community of designers who are using nonlinear circuit simulators with good success to design and optimize high-power amplifiers. For this simulation-based design community, the success of their PAs, whether for wireless communications or military applications, depends on the accuracy and scalability—with bias, temperature, and geometry—of available nonlinear models for power transistors.

At a top level, one might ask questions like "Nonlinear FET models for PA design have been available for some time now, so why are we still talking about them?" and "Isn't this a solved problem?" The reality is that the demand and requirements for more accurate nonlinear models in new and existing devices continues to increase. In fact, it is common knowledge in the industry that the lack of a good nonlinear model can be a significant impediment to having a commercial GaN device considered for new designs.

With this demand has come an accompanying need for advanced model testing. For example, as operating power increases, thermal issues play a larger role and pulsed measurements are required to either avoid variable self-heating during testing or to help keep the device at a safe temperature during the intended operation. Load-pull measurements are certainly in the category of advanced model testing. These measurements include straightforward single-tone power compression and efficiency optimization, to two-tone and multitone distortion testing, amplitude modulation/phase modulation (AM/PM) load-pull and pulsed radio frequency (RF)/pulsed bias load-pull testing. Also, time domain waveform measurements and nonlinear network analyzer measurements are being increasingly applied to the problem of nonlinear power transistor model validation.

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Digital Object Identifier 10.1109/MMM.2010.937735

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Among the considerations for good power transistor models are the overall measurement accuracy, the suitability of the model, and the types of validations executed to test and refine the model. Fixturing and calibration methods/standards play a very important role in achieving an accurate data set to use for models; after all, compact model accuracy starts (and can stop) with data accuracy. In this article, we discuss modeling considerations for GaN HEMT devices and nonlinear modeling techniques that can predict the particular behaviors of GaN devices. We will review several popular compact FET models including commercially available models as well as the in-house models discussed in the next section. This treatment expands the presentation of GaN modeling considerations given at a recent conference [10].

A Tour of GaN HEMT Modeling Work

A review of the microwave device modeling literature reveals that much work has been done in the area of nonlinear modeling in the context of GaN HEMT treatment. Most of this work is targeting accurate measurement-based compact models that can be used for design work. Such models are implemented in simulators variously as C-code, Verilog-A code, and as symbolically defined devices (SDDs) among other coding approaches. Figure 1 shows a nonlinear equivalent circuit topology used in the most recent model by Angelov et al. [11]. As will be explained in the next section, element values and equation fitting coefficients are extracted or optimized to provide a best fit to various measured data.

Various available GaN HEMT compact models differ somewhat in topological details, but, more significantly, they are distinguished by the equations used to fit the voltage-dependent I_{DS} and the functions used to represent the voltage dependent capacitance or charge representations of C_{gs}, C_{gd}, and C_{ds}. Most popular models have electrothermal models that consist of an equivalent electrical analog thermal resistance R_{therm} and capacitance C_{therm}, as depicted in Figure 1. These electrothermal models provide a means to estimate the channel temperature rise due to dc power dissipation. The one shown is a simple single pole model, which can be expanded to address multiple thermal time constants if needed to represent more complex behavior.

To better understand the foundation for GaN HEMT compact models, most of the reported work represents either a straightforward application of compact models originally developed for GaAs metal–semiconductor field-effect transistor (MESFETs) and HEMTs or extensions to and customizations of such models. These well-established models include the original Curtice model [12], the Eesof GaAs HEMT (EEHEMT) model [13], and the original Angelov-Chalmers model [14], which is also referred to as the *Angelov* model or the *Chalmers* model.

The EEHEMT model is itself an extension of the Curtice model. The EEHEMT model separates the dc and ac behavior for a simpler model extraction. However, this makes complex time-dependent thermal effects in the in-between or low-frequency region (where temperature can vary with the ac signal fluctuations) more difficult to characterize. The model reported by Camarchia et al. [6] uses the original Curtice model as the basis for a

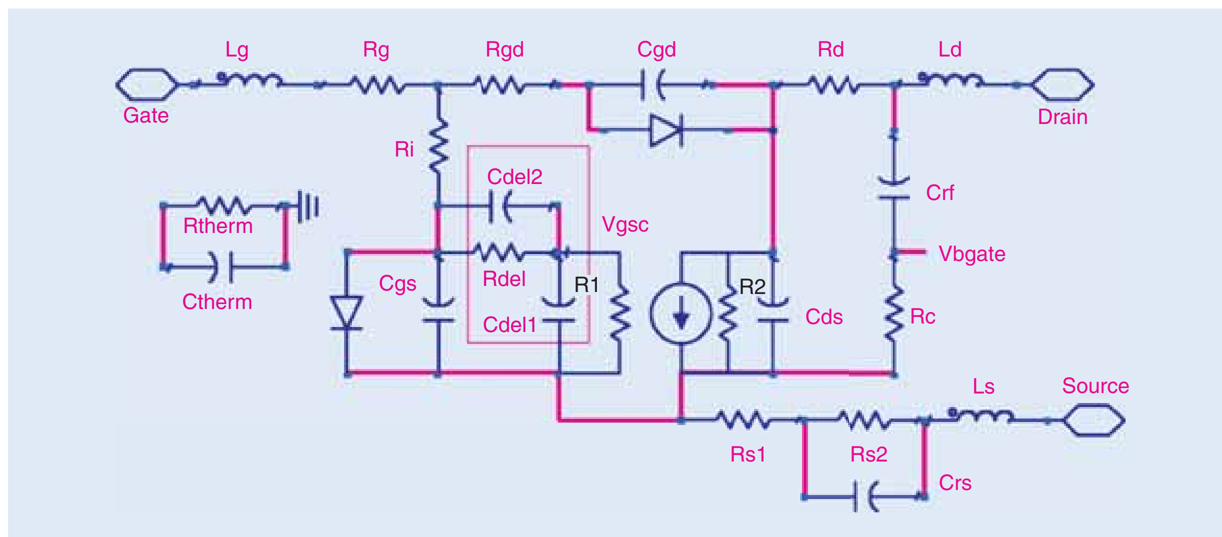

Figure 1. *Topology for the Angelov GaN HEMT model [11]. The electrothermal model elements Rtherm and Ctherm enable estimation of channel temperature rise due to power dissipation.*

comprehensive so-called self-consistent electrothermal model. This model is developed by fitting a behavioral thermal equivalent circuit model to this analysis. Results are shown for a GaN HEMT device, illustrating the impact of improved electrothermal modeling on memory effects such as variations in third-order intermodulation power (IM3) with tone spacing. Kharabi et al. report good success with the EEHEMT model for modeling the RF Micro Devices, Inc. (RFMD) GaN devices [15]. Curtice has expanded considerably on the original model of [12] with present model variations called *CFET* and *C_HEMT* (with the most recent versions of these labeled *CFET9* and *C_HEMT3*, as of this writing). These models have specific enhancements that aid with GaN modeling [5]. The separate works of Casto and Dooley [7] and Lee and Webb [8], [9] both report good results using the CFET model for GaN modeling.

Updates have also been made to the original Angelov model and there is now a GaN-specific version (termed *Angelov_GaN*) available in Verilog-A code. This updated model has the topology of Figure 1 and is the basis for the work reported in Angelov, et al. [16] and Angelov, et al. [11]. The Angelov_GaN model includes modifications to the Ids model to address improved prediction of harmonics as well as g_m and g_{ds} dispersion. Modifications are also made to better assure charge conservation of capacitance functions. Another model that has been demonstrated to be effective for GaN HEMT modeling is the Auriga model discussed by Tajima [4], which is reported to be a significant expansion to the Angelov model. The original Angelov model has also been used by the authors of this article with good success, and it has also been modified to add bias and geometry scalability. Results from this model will be discussed later.

Among the considerations for good power transistor models are the overall measurement accuracy, the suitability of the model, and the types of validations executed to test and refine the model.

Two models that have used a common but different starting point for their current formulation are that of the in-house model presented by Cabral et al. [17] and the proprietary Cree model, as described by Pengelly et al. [18]. Both of these groups start with the current formulation of Fager et al. [19]. This formulation was originally developed for silicon LDMOS transistors. Cabral et al. provide a compelling example of how Fager's four-region current formulation leads to improved comparison to measured data in terms of the derivatives of the current functions (for example, gm, gm2, and gm3), when compared to the original Angelov model [14]. Both Pedro et al. and Pengelly et al. report improved third-order intermodulation distortion and spectral spreading prediction with their models compared to the more established MESFET/HEMT formulations.

Nonetheless, the example of Figure 2, which was provided by coauthor Walter Curtice, suggests good results can be achieved for third-order effects, such as IM3 and third harmonic power with the Angelov model. Shown is a comparison to an EEHEMT model for the same device, which, in this particular case, shows improved third harmonic prediction for the Angelov model. However, we will later show a different GaN HEMT example where third-order IM3 was predicted quite acceptably with an EEHEMT model.

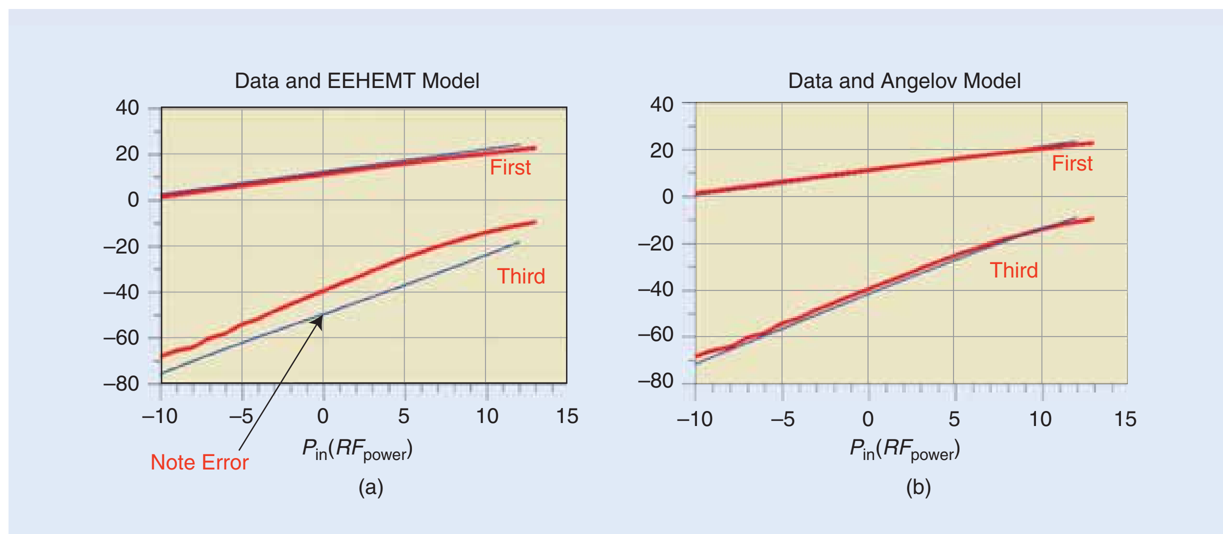

Figure 2. *Comparison of fundamental and third harmonic output power for a 1.75-mm GaN HEMT device. (a) EEHEMT model fit. (b) Angelov model fit. Measured data are red and modeled results are blue.*

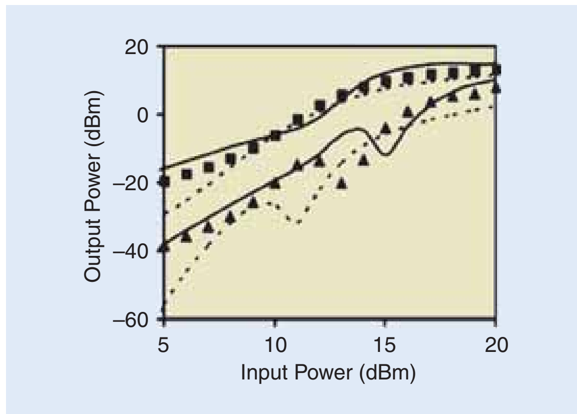

Figure 3. *Measured (symbols) third-order (top curve) and fifth-order (bottom curve) intermodulation distortion of a Class-A amplifier under optimum source and load matches at 1.9 GHz versus that simulated with Angelov (—) and EEHEMT (- - -) models for a GaN MOSHFET device [20].*

Another example of an Angelov-based model providing good intermodulation distortion prediction for GaN devices is shown in the work of Deng et al. [20], wherein modifications were made to the Verilog-A code version of the Angelov model to tailor its applicability to metal–oxide–semiconductor heterostructure field-effect transistor (MOSHFET) devices, which are similar to GaN HEMTs with the exception of a thin oxide layer that is introduced as a gate insulator having the positive effect of reducing gate current. Figure 3 shows measured and simulated IM3 and IM5 for a Class AB amplifier based on a modeled GaN MOSHFET device. Simulated results are shown for both the modified Angelov model and an EEHEMT model for the GaN device.

To put the examples of Figures 2 and 3 in some perspective, the work of Pedro et al. [17] specifically focused on making sure third-order effects were properly modeled. Other models, with appropriate attention, may or may not give acceptable results for third-order distortion and harmonic results. It is misguided to assume that they will without adequate advanced model testing and careful validation at or near the operating region of interest.

Recent publications also include those specifically addressing the often significant trapping effects in GaN HEMTs as well as numerical approaches. Examples of this work include the drain-lag model described by Jardel et al. [21], along with the treatment of Baylis that modified the Angelov current formulation to address quiescent-bias dependent trapping effects [22]. Physics-based numerical modeling approaches [3], [23] have revealed much new understanding of effects that need closer attention, such as breakdown behavior and the aforementioned nonlinearity of the GaN HEMT source resistance.

Table 1 is a summary of various FET models, which includes models that are being used for GaN HEMT transistors. Also included for comparison purposes are selected models used for GaAs MESFET, silicon MOSFET, and LDMOS devices. Models with a larger number of parameters are not necessarily better for a given task, but, generally speaking, are set up with additional parameters to either tie the model more closely to physical process effects, as in the case of the Berkeley Short-Channel IGFET Model (BSIM) type of models [24], or to have increased flexibility in modeling specific ac and dc aspects of the device behavior, as is the case with the EEHEMT model. The following are a few reasons why a lower number of parameters are desirable:

- Model parameter extraction time increases with the number of parameters. A 100-parameter model takes considerably longer to extract than a 50-parameter model.

TABLE 1. Comparison of example FET models used for GaAs, silicon, and GaN FET/HEMT devices.

FET Models	Approx. Number of Parameters	Electrothermal (Rth-Cth) Model	Geometry Scalability Built-In	Original Device Context
Curtice3 [12]	59	No	No	GaAs MESFET
Motorola Electrothermal (MET) [25]	62	Yes	Yes	LD MOSFET
CMC (Curtice/ Modelithics/Cree) [26]	55	Yes	Yes	LD MOSFET
BSIMSOI3 [24]	191	Yes	Yes	SOI MOSFET
CFET [5]	48	Yes	Yes	HEMT
EEHEMT [13]	71	No	Yes	HEMT
Angelov [14]	80	Yes	No	HEMT/MESFET
Angelov GaN [11]	90	Yes	No	HEMT
Auriga [4]	100	Yes	Yes	HEMT

- The parameters of a large parameter set model tend to be less physical and more empirical.
- Uncertainty in parameters increases greatly as the number of parameters increases. This can cause poor convergence in optimization routines.

It should also be noted that even though all models shown have temperature dependences built in to the equations, not all have full electrothermal models that address self-heating. Self-heating is caused by average power dissipation in the device. The self-heating varies with dc bias and, at high power, with RF signal levels. Most of the models listed are commercially available as built-in models in microwave circuit simulator, such as Agilent Advanced Design System (ADS) and Applied Wave Research (AWR) Microwave Office. The Angelov model is also available in Verilog-A format in both the original [14] and Angelov_GaN [11] versions. The CFET model can be purchased from W.R. Curtice Consulting as add-on software. The Auriga model may be accessed through commercial model extraction services offered by Auriga Microwave. With the exception of this model, Modelithics offers extraction services for the other models listed. Relatively speaking, the Angelov model parameter extractions tend to be more time-consuming in comparison to EEHEMT and CFET, for which IC-CAP routines are readily available to assist with the extraction process.

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Basic Modeling Strategy, Considerations and Issues

The following discussion presents a nonlinear characterization and modeling strategy in the context of addressing some of the specific issues relevant to GaN modeling. A typical test station used to acquire data for model coefficient extraction consists of a wafer probe station, broadband vector network analyzer (VNA), dc and pulsed current voltage (*I*–*V*) analyzers, and a computer-running software that facilitates at least instrument control and data acquisition if not also model extraction [13]. A typical nonlinear transistor modeling process is outlined in Figure 4. The reader is referred to one of the texts available for more detailed transistor modeling information [27]–[29].

As a first step, *I*–*V* and multibias S-parameter measurements (often pulsed) are performed. Understanding trapping effects and their bias dependence is important for successful GaN HEMT modeling. Here judicious application of pulsed *I*–*V* techniques is recommended. Pulsed *I*–*V* techniques began in the FET modeling context with the groundbreaking work of Platzker et al. [30]. The introduction of commercially available systems greatly facilitated such applications, and pulsed *I*–*V* measurements are now used for routine model extractions as well as research. Commercial pulsed *I*–*V* measurement systems have been developed by the manufacturers such as

- Agilent Technologies
- Accent Optoelectronics
- Auriga Measurement Systems
- Keithley Instruments
- Focus Microwaves
- AMCAD.

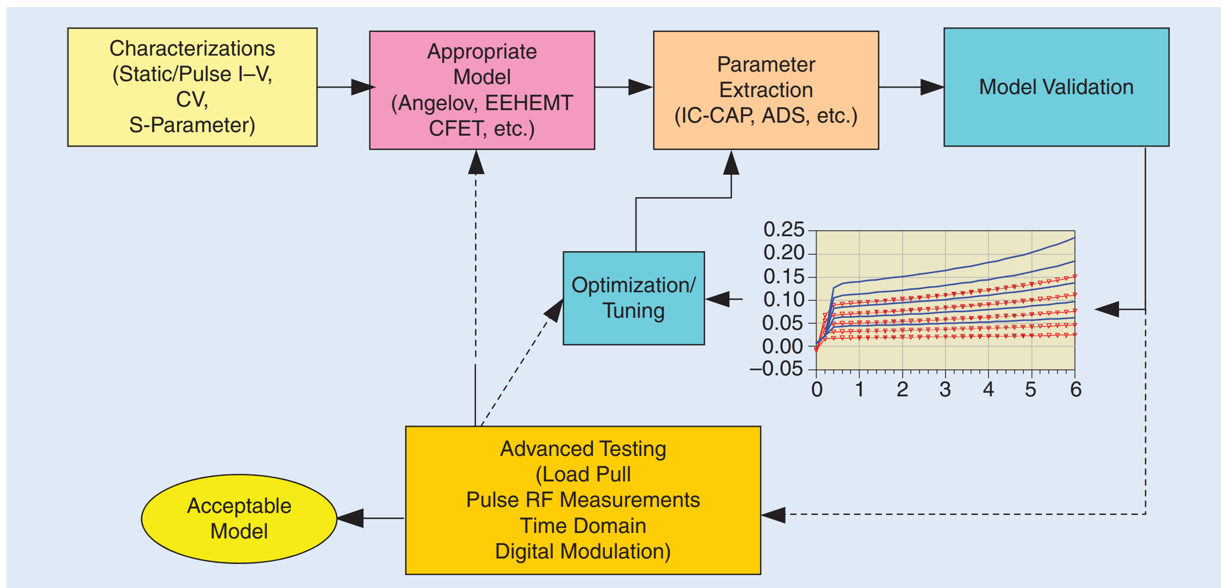

Figure 4. *Nonlinear transistor modeling process.*

GaN HEMTs often show a significant quiescent-bias dependence in their operating characteristics.

Some of the original systems have been made obsolete by their manufacturer but their systems are still in active use in modeling laboratories. The Auriga AU4750 illustrated on the left side of Figure 5 is an example of a commercially available pulsed *I–V* test system.

Pulsed *I–V* analysis has been applied by many to understand trapping effects in III-V devices, including the original GaN trapping origins and its characterization [1], [31], [32]. For the case of GaN HEMT modeling, pulsed *I–V* measurements are effective for extracting an isodynamic equation for I_{DS}. The term *isodynamic* is used when thermal and trap conditions are held at values corresponding to the specified quiescent bias condition. This is in comparison to a static *I–V* measurement, representative of a traditional curve tracer or dc parameter analyzer, where acquisition of each data point is slow enough that traps, if present, and thermal conditions can be different at each of the acquired data points. Figure 6 shows a comparison of pulsed and static *I–V* measurements for a GaN transistor [22], where the thermal heating effects in the high $V_{ds} * I_{ds}$ power dissipation region are quite clear in contrast to the isodynamic pulsed *I–V* data. Typical pulsed *I–V* conditions might consist of 0.1 to 0.5 μs pulse widths, separated by time intervals on the order of 1 ms. These data were acquired using an Accent Optoelectronics DiVA instrument.

GaN HEMTs often show a significant quiescent-bias dependence in their operating characteristics. As an illustrative example, pulsed *I–V* measurements made by Baylis [22] are shown in Figure 7. In this figure, *I–V* curves from several different values of zero power dissipation quiescent bias conditions are shown. In Figure 7(a), the quiescent drain-to-source voltage V_{dsQ} is held at 0 V while the quiescent gate-to-source voltage V_{gsQ} is varied from −5 V to 0 V. In Figure 7(b), the gate voltage is held at threshold, such that the drain current is zero and the drain voltage (V_{dsQ}) is varied between 0 and 4.5 V. Because the power dissipation (based on the quiescent bias) is zero for all of the measurements, the variations observed in both plots are due only to trapping effects and not thermal effects. Baylis introduced modifications of the original Angelov current equations that allow for such quiescent

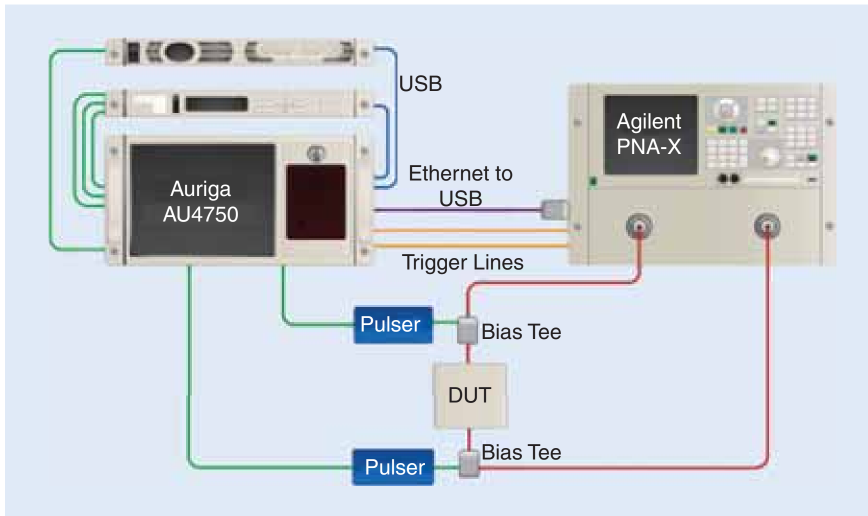

Figure 5. *Commercially available setup for pulsed I–V and pulsed S-parameters. (Courtesy Auriga Microwave, used with permission.)*

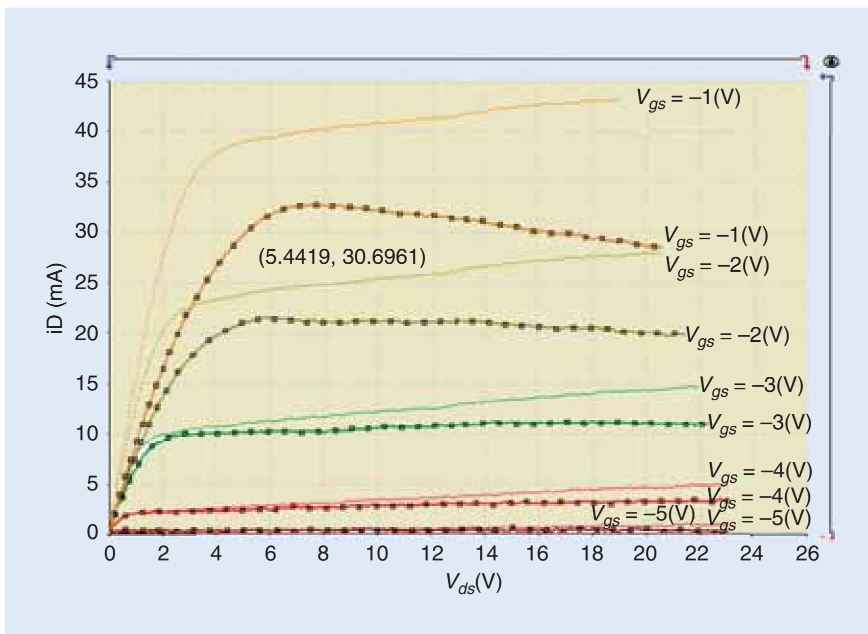

Figure 6. *Comparison of pulsed I–V (solid lines without symbols) and static I–V for a GaN HEMT. Pulse conditions were 0.2 μs pulse width and 1-ms separation with quiescent bias set at $V_{dsq} = 0$, $V_{gsq} = 0$. V_{gs} is varied from −5 to −1 V in 1 V steps.*

bias-dependent trapping effects in I–V curves to be captured in a nonlinear model. It should be mentioned the device represented in Figure 7 is a noncommercial device with significant gate- and drain-dependent trapping. Commercial devices with quality surface passivation will show much less gate-dependent trapping and may show a less pronounced current collapse than illustrated here. Nevertheless, for GaN modeling it is important to make sure that pulsed I–V measurements are used for model fitting with the quiescent bias point to be at or near the desired operating bias point(s).

Zero V_{ds}-biased cold-FET S-parameter measurements are generally performed to assist with nonbias-dependent extrinsic parasitic element determination. Referring to Figure 1, Ld, Lg, and Ls, along with extrinsic resistances and pad capacitances (if present and significant), for example, would all be determined in this way. If the device is packaged, package parasitics will also need to be modeled and de-embedded from the measurements. The same strategy used for LDMOS packaged device modeling [28] can be applied to separate package parasitic and intrinsic device model aspects for GaN HEMTs. Preferably, both chip and packaged versions of the device are available, as it is better to model the intrinsic device using chip-level data.

Capacitance-voltage (CV) behavior is most often derived from multibias, hot-bias S-parameters after extrinsic element effects have been de-embedded from the measured data. The selection of the model will be driven by a number of considerations, including availability of the model and extraction tools in the chosen circuit simulator. For maximum flexibility, one advantage of having a model available as either a symbolically defined device

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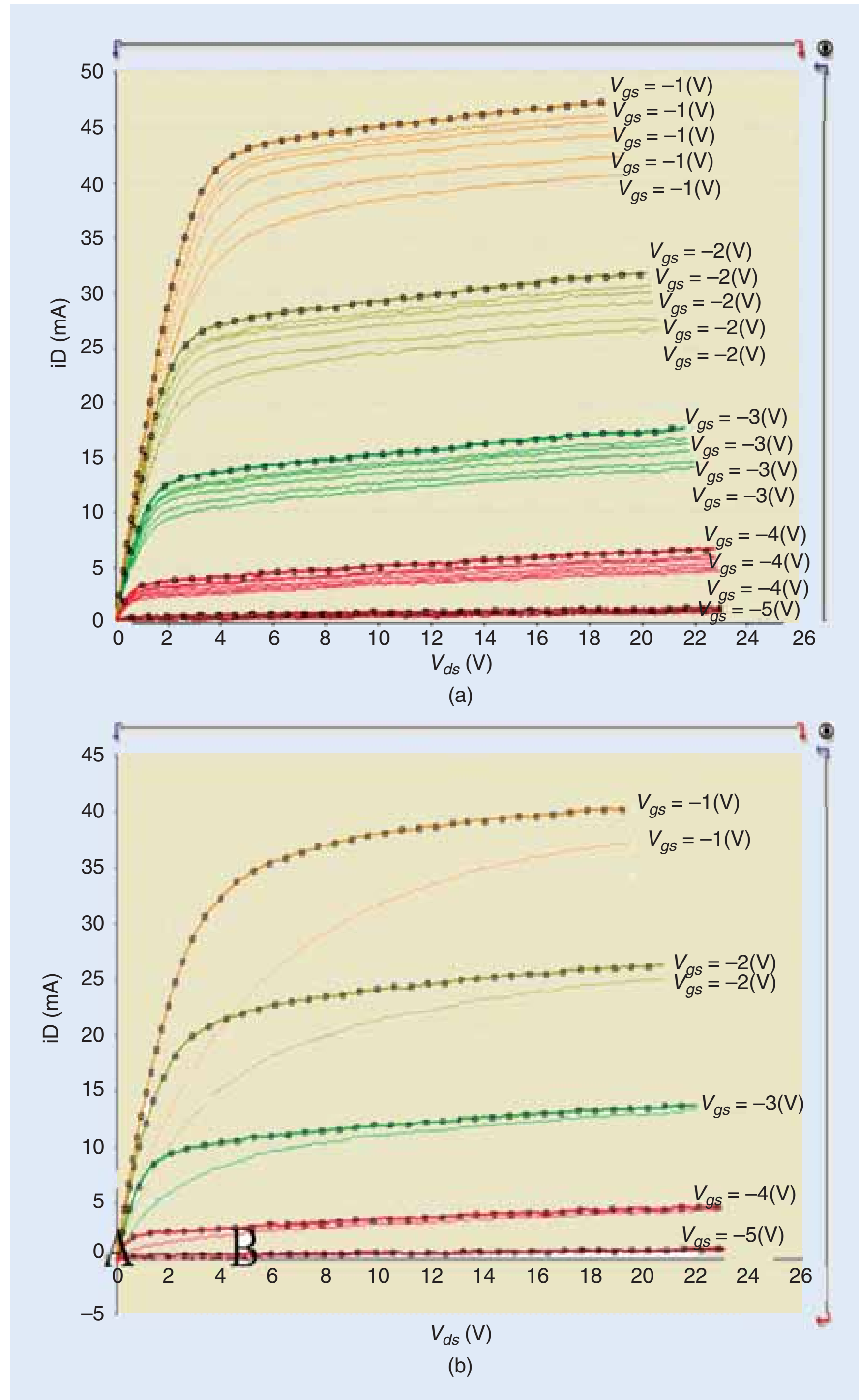

Figure 7. *Bias dependent trapping effects for a GaN HEMT. In all cases, the dc power dissipation is zero as pulsing is either from (a) $V_{ds} = 0$ and various V_{gs} values and (b) $V_{gs} <$ pinchoff and varied V_{ds}. Pulse conditions were 0.2-μs pulse width and 1-ms separation. V_{gs} is varied from −5 to −1 V in 1 V steps.*

Pulsed S-parameter measurements additionally can be used to ensure that the correct thermal dependences of the model's capacitance equations are extracted.

or Verilog-A code is that modifications to the model can be made if necessary to better track observed voltage dependences. As powerful as the models described in the prior section can be, compact models are still empirical approximations that cannot fully capture all the effects of a real physical device for all operating regions and conditions [33].

Once the appropriate model is selected, model parameters are extracted using software such as Agilent IC-CAP and/or utilizing a circuit simulator like ADS or AWR Microwave Office. The model is then validated, often with emphasis on the important regions for the targeted application. That is to say, as a general rule, nonlinear models do not necessarily work well globally at all possible quiescent bias conditions. Rather, it is common to focus on a particular operating region when fitting model parameters. For example, for Class E applications, special attention is given to fitting *I*–*V* and S-parameters in the threshold and knee regions. As pointed out by Negra et al. [34], a model developed for Class AB may not be effective for Class E/D switched-mode applications. However, the particular model reported by Negra et al. appears to be limited in application to subgigahertz applications. In contrast, we have found that good results can be achieved for modeling Class E type devices by focusing attention on making sure the model fits well in the threshold (zero current) off and knee on regions with models such as the EEHEMT and the CFET.

Turning attention to the electrothermal circuit of Figure 1, a number of useful measurement techniques to extract thermal resistance and time constants, or thermal capacitance, have been demonstrated for silicon devices that possess minimal trapping effects [35]–[38]. Casto and Dooley [7] applied similar methods to extract an electrothermal model for GaN HEMTs by performing pulsed *I*–*V* and S-parameter testing at multiple temperatures and biases and validating results against infrared measurement results. As mentioned earlier, another group has demonstrated the usefulness of numerically based thermal analysis as part of their electrothermal modeling strategy [6].

Pulsed S-parameter measurements additionally can be used to ensure that the correct thermal dependences of the model's capacitance equations are extracted. These differences are caused by self-heating effects as well as electron emission and capture by trap states on the surface and in the substrate of the device. More effort and model complexity is required if the goal is to have a model that can scale accurately with geometry and/or with quiescent bias conditions. As with pulsed *I*–*V* measurements, pulsed bias S-parameters are pulsed from one specific quiescent bias point at a time.

When performing pulsed bias/pulsed S-parameters, careful attention needs to be paid to the bias tees used, as the frequency and time-domain step response of the dc bias path can severely limit the pulsed conditions that can be used [39]. Figure 8 shows examples of a pulse response of the dc to RF + dc port of both an example commercial bias

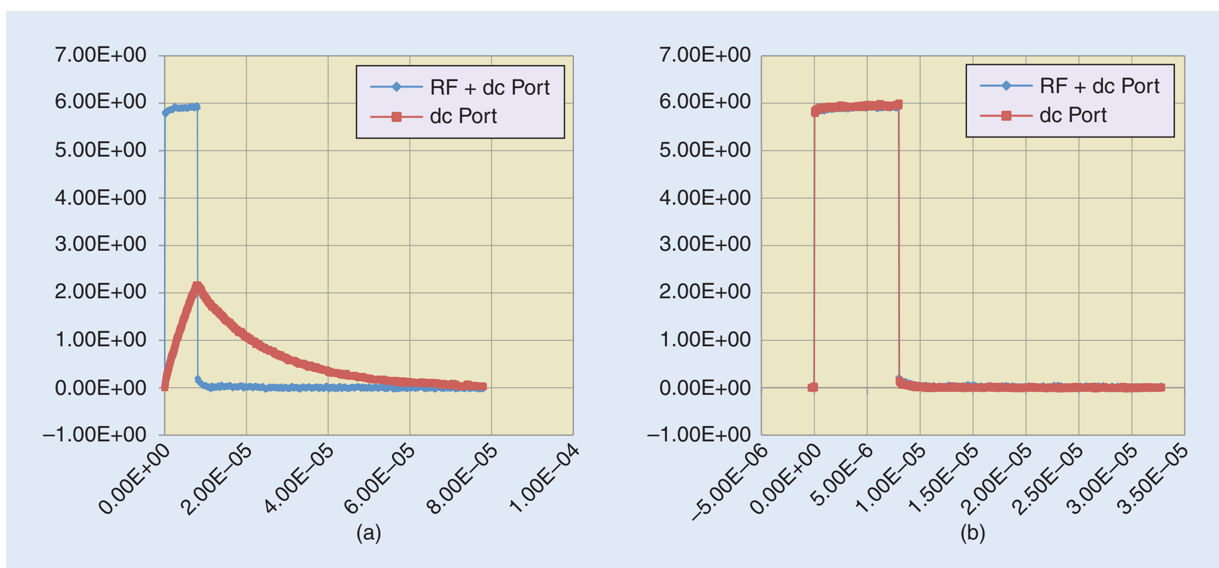

Figure 8. *Pulse width 8 μs and period 80 μs (10% duty cycle) for (a) a commercial bias tee and (b) a custom in-house bias tee. Note: The y-axis is voltage and x-axis is time in seconds for both plots.*

tee [Figure 8(a)] and a custom in-house bias tee [Figure 8(b)]. For pulsed S-parameters, the VNA measurement approach can also limit the measurement dynamic range depending on the pulse width and/or duty cycle [40]–[42].

The commercially available system shown in Figure 5 enables both pulsed *I–V* and pulsed S-parameter measurements by combining the Auriga AU4750 pulsed *I–V* system with an Agilent PNA-X network analyzer. An example of a comparison of pulsed and static bias S-parameters for a GaN HEMT made with this system is shown in Figure 9, where the effects of self-heating for the static-bias case are exhibited as a gain drop of about 1–1.5 dB. In addition to addressing self-heating and trapping issues, pulsed S-parameters allow data to be taken in regions where the device may fail due to overheating. While pulsed S-parameters are clearly useful for many large-signal device modeling applications, it should also be noted that the authors have developed nonlinear models over the past several years for a multitude of power devices without the use of pulsed S-parameters. Positive feedback from designers using these models as well as load-pull validations has confirmed the accuracy of the models so derived.

In referring to Figure 4, much of the model parameter extraction and fitting for GaN HEMTs is performed using *I–V* and S-parameter data and it is the advanced testing area "where the rubber meets the road," so to speak, for a given application. Application-specific testing that is tailored to the given application can help reveal whether the model can meet the demands of the target design type, or help to identify how to further refine the parameter set to make sure the model can be useful for the type of PA design for which it is intended. Single-tone scalar load- and source-pull testing is done at a minimum. Depending on the final circuit application for which the model is intended, load-pull validation requirements may, in

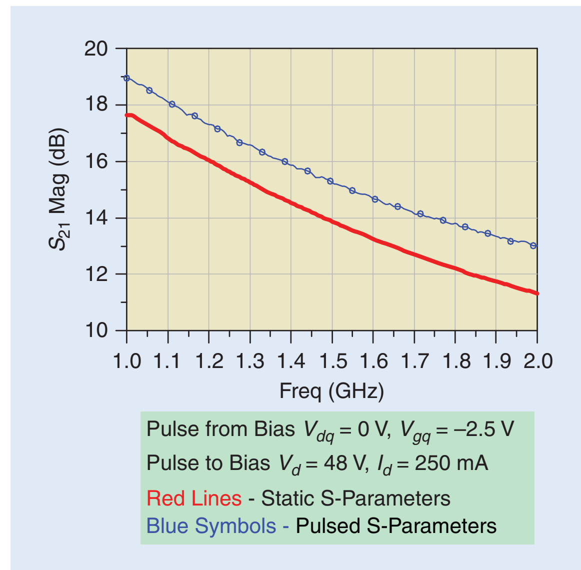

Figure 9. *Pulsed S-parameter and static S-parameter comparison for a 10 W GaN HEMT. Pulse conditions: 5 μs pulse width, 0.1% duty cycle (IF BW = 1/pulse width = ~200 kHz).*

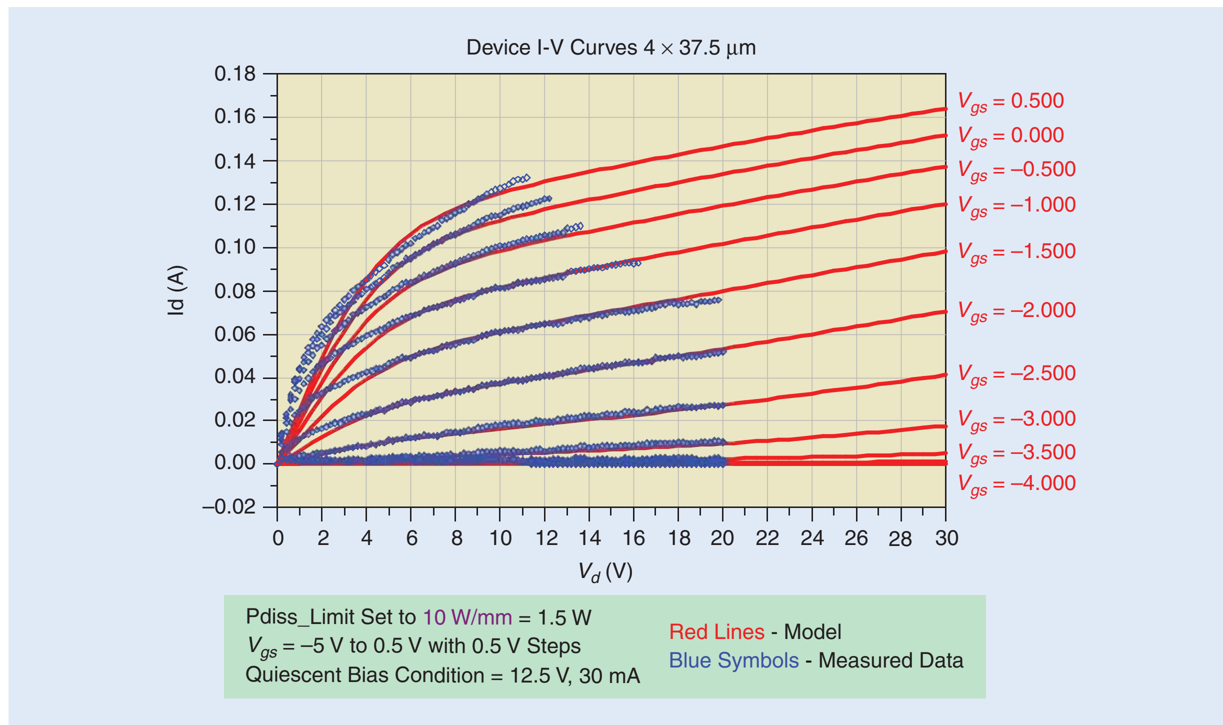

Figure 10. *The 25 °C pulsed I–V curves for a 4 × 37.5 μm GaN HEMT device compared to an extracted EEHEMT model.*

many cases, expand to include two-tone linearity testing, harmonic impedance, AM/PM, adjacent channel power ratio, and error vector magnitude as well as time-domain waveform testing. Advanced testing validations of GaN device models these days increasingly are including tests like large-signal network analyzer or nonlinear VNA-measured waveforms tested under varied fundamental and harmonic load-pull conditions.

In summary, a large amount of work has been applied by several groups to develop and test the capabilities of various model topologies and equation sets for use in GaN HEMT modeling. Other areas needing careful attention in extracting trustworthy models for GaN HEMTs include obtaining appropriate and accurate sets of characterization data, with attention paid to thermal and trapping effects, along with extensive large-signal (or advanced testing) validation.

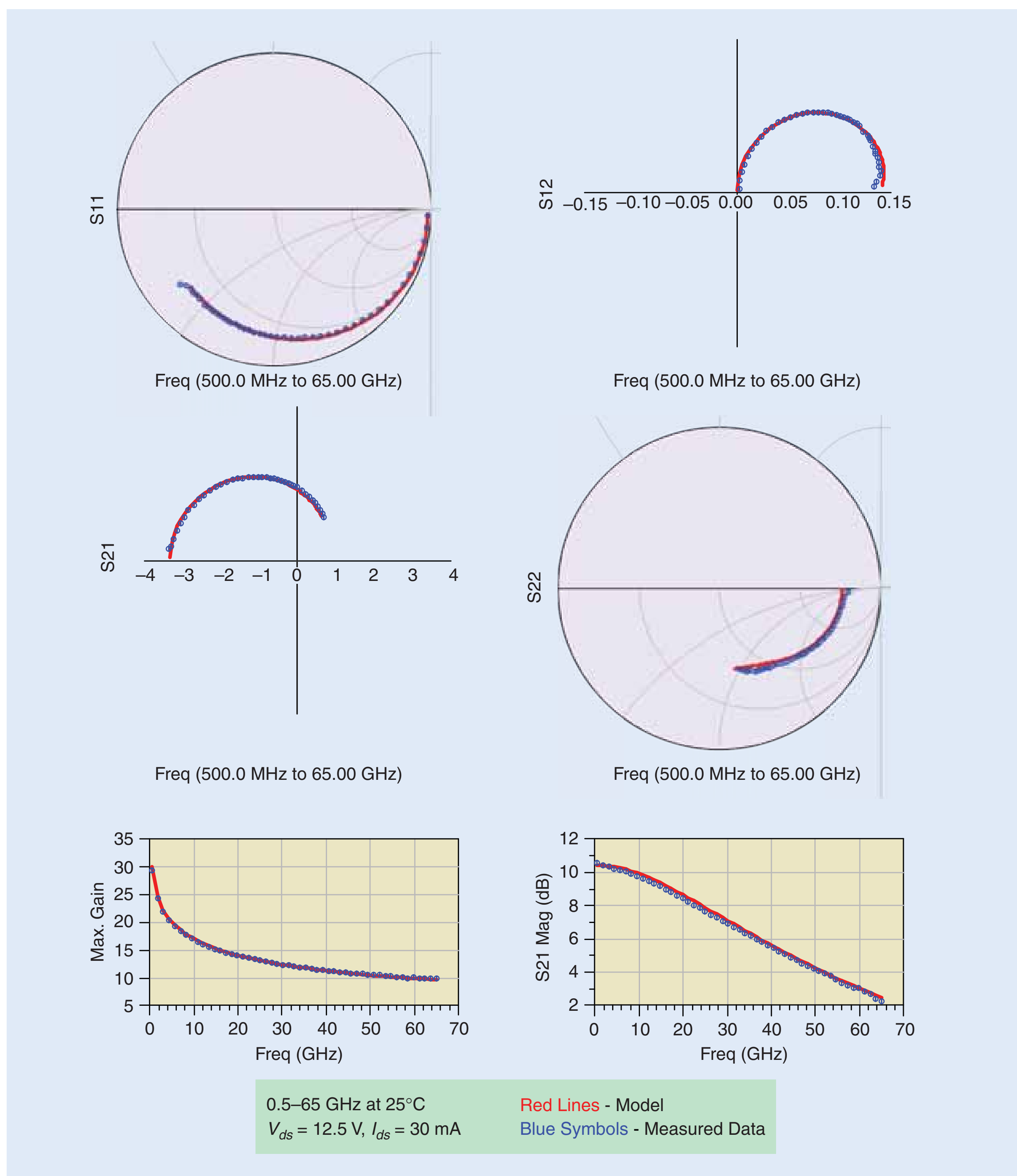

Figure 11. *The S-parameter comparison for a 4 × 37.5 μm, GaN HEMT device.*

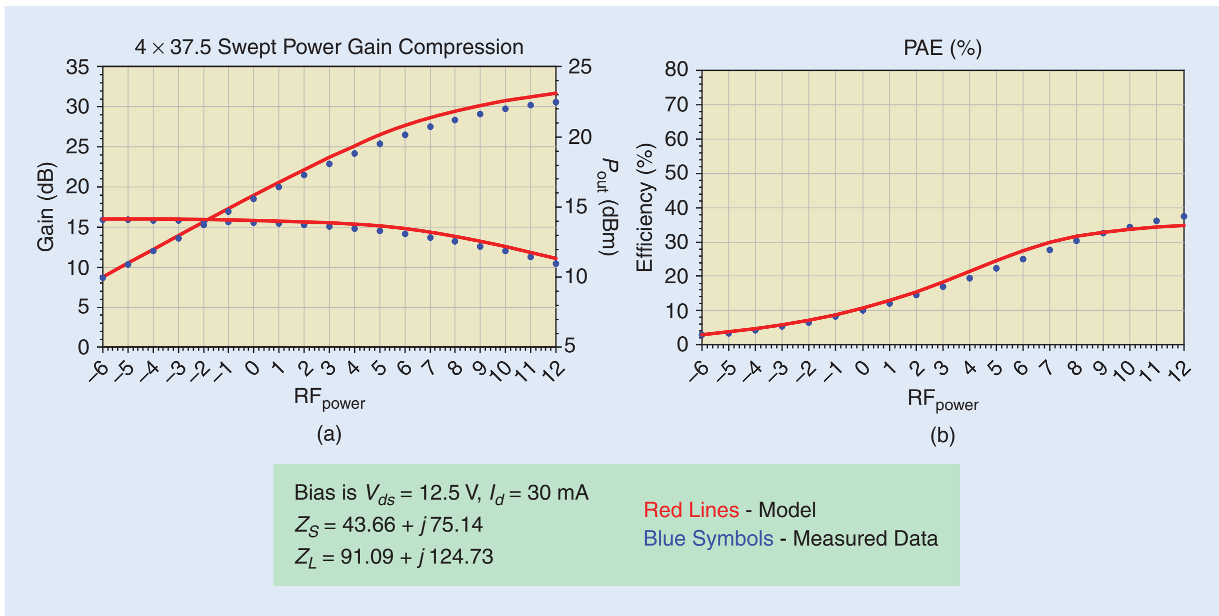

Figure 12. *The 17-GHz power-tuned swept-power comparison of an EEHEMT for a 4 × 37.5 μm GaN HEMT device.*

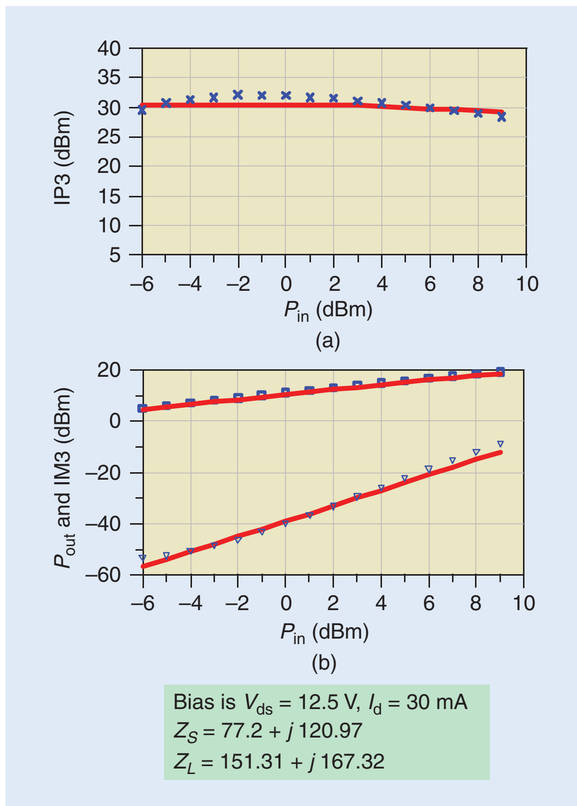

Figure 13. *The 17-GHz IP3-tuned swept-power comparison of an extracted EEHEMT model (red line) and measured data (blue symbols) for a 4 × 37.5 μm GaN HEMT device.*

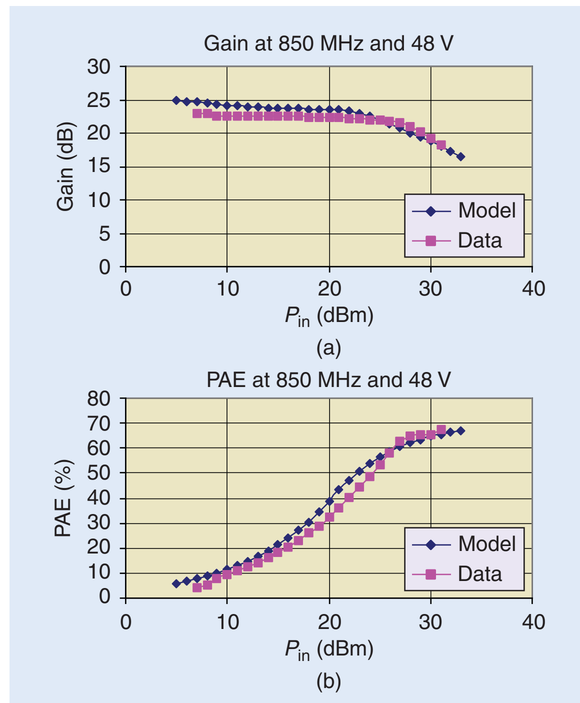

Figure 14. *(a) Gain and (b) power-added efficiency (PAE) for a 45-W packaged GaN HEMT versus input power for f = 850 MHz, VDS = 48 V, ZS = (2.046 + j1.960) Ω, and ZL = (6.857 + j5.7) Ω. This device was modeled with a Curtice FET model.*

Example Modeling Results for GaN HEMT Devices

Next we will turn our attention to several example models for GaN HEMTs of various sizes. All the model examples presented in this section have been extracted by Modelithics, starting with an EEHEMT model example. Figures 10–13 show modeling results for a relatively small 4 × 37.5 μm gate width geometry GaN HEMT chip intended for milimeter-wave applications. Figure 9 shows the *I–V* curve is

With the powerful benefits of GaN devices, unique challenges are encountered as a result of trapping effects, related current collapse, high voltages and currents, and corresponding thermal issues.

reasonably well fit to measured data, with some differences observed in the knee region. Figure 11 shows a very good fit for all four S-parameters for this same model through 65 GHz. Figure 12 demonstrates that the model fits single-tone power-swept gain and efficiency very well after the completion of a load-pull measurement at 17 GHz. Figure 13 indicates that it is possible to obtain good fits to third-order distortion measures with the EEHEMT model. The third-order intercept point (IP3) and third-order intermodulation levels are well predicted by the model extracted for this particular device. Moving on to a much larger device, Figure 14 shows favorable comparisons for an extracted CFET model for a 45-W packaged GaN HEMT device. Shown are swept power gain compression and efficiency comparisons made at optimal termination conditions determined from load-pull testing at 850 MHz.

As a final example, an Angelov model was extracted for a 10-W transistor and scaled to represent a 100-W

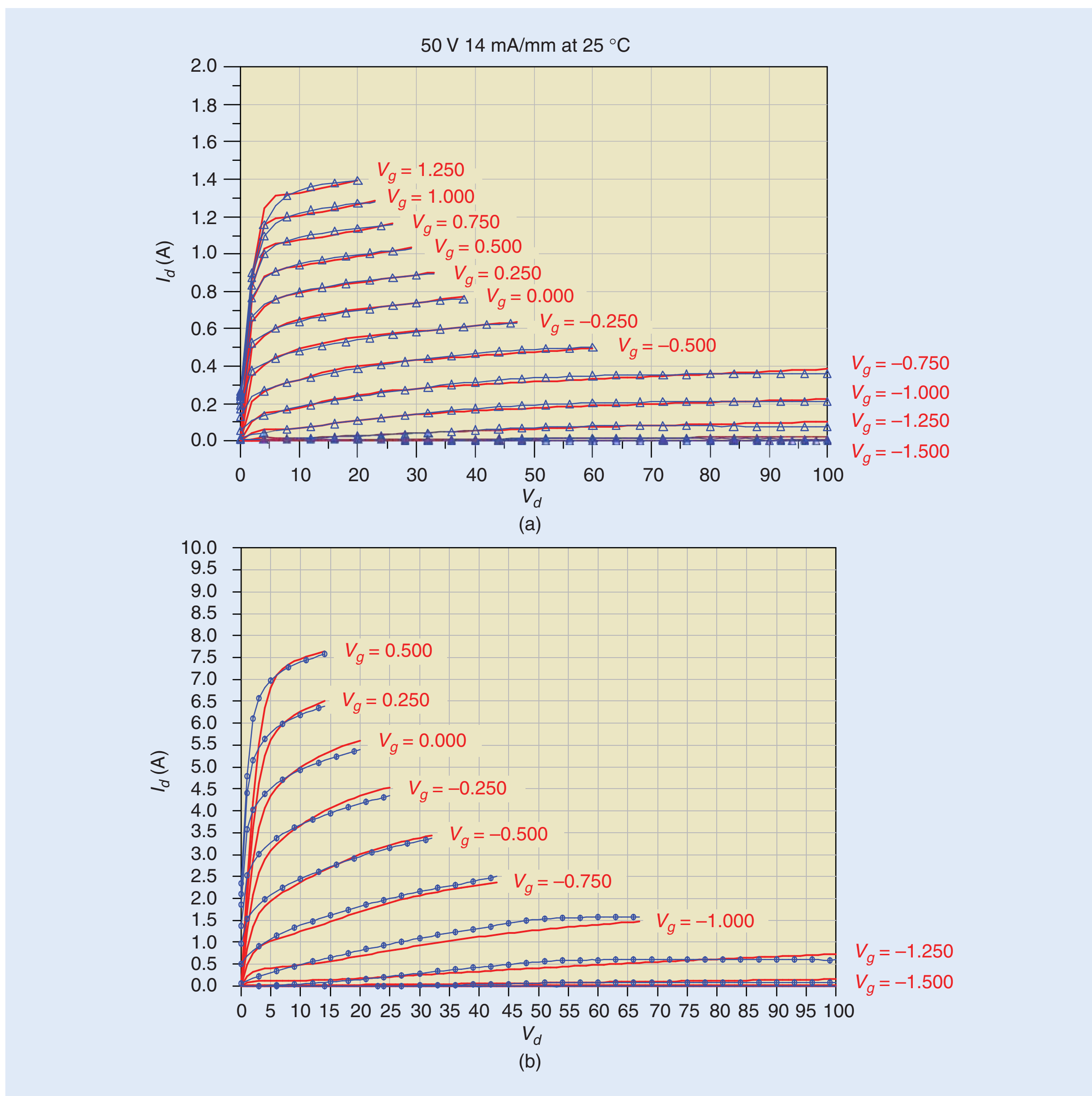

Figure 15. *Pulsed I–V measured and simulated data for 10 W and 100 W chip-level GaN devices. Quiescent bias for both pulsed I–V sets is V_{ds} = 50 V and $I_{ds} \sim 0$. Pulse width was 0.2 μs.*

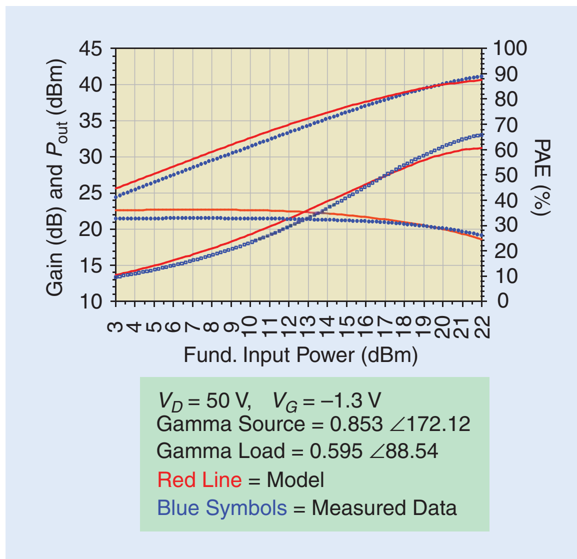

Figure 16. *25 °C power tuned power sweep for the 10 W unit cell GaN transistor measured at 2.14 GHz.*

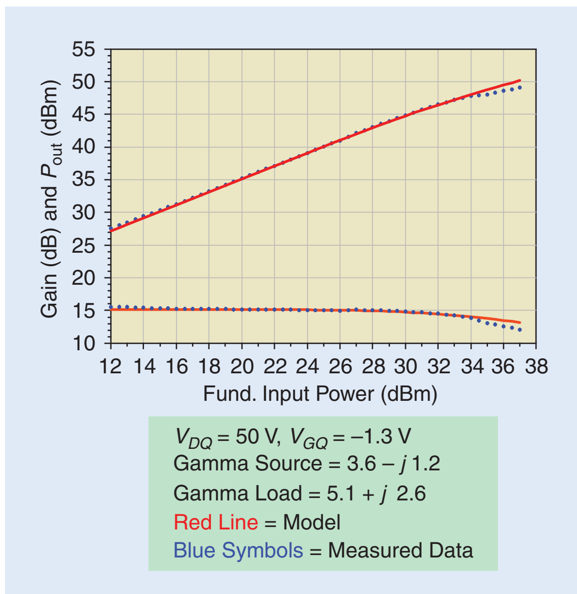

Figure 17. *2.14 GHz swept-power measurement of a 100 W GaN transistor compared to simulations with Modelithics scalable GaN model. Data is taken under pulsed conditions with 80 μs pulse period, 80% duty cycle.*

transistor. The model used incorporates in-house quiescent bias and geometry scaling. The same model is used for all results shown, with only a change in scaling factors or quiescent bias included. Figure 15 shows pulsed *I–V* results for both devices, demonstrating a very good *I–V* fit over the entire operating region for both data sets. Figure 16 shows power-swept results after load-pull was performed on the 10 W transistor at 30 V, while Figure 17 demonstrates good agreement for simulations compared to pulsed load-pull results for the 100 W GaN data.

Conclusions

With the powerful benefits of GaN devices, unique challenges are encountered as a result of trapping effects, related current collapse, high voltages and currents, and corresponding thermal issues. This article has reviewed recent modeling work focused on addressing GaN modeling challenges along with strategies for successful measurement-based modeling of GaN transistors. The use of pulsed measurements as part of the modeling process, along with sufficiently flexible modeling equations and topologies, is critical for obtaining reliable electrothermal GaN models. In addition to the model extraction measurements of *I–V* and multiple-bias S-parameter data, large-signal measurements (load-pull, power sweep, linearity, and waveform) are also a critical part of model validation and improvement. Excellent model results can be obtained with suitable in-house models or by using established HEMT models available for popular microwave nonlinear circuit simulators. Examples are shown for accurate GaN models developed using the EEHEMT, CFET, and Angelov modeling templates. A given model's effectiveness will vary with the skills of the measurement and modeling team along with applications and power amplifier operating modes. The successful modeler will be aware of the need for accurate data, carefully applied extraction methodologies, along with the strengths and limitations of available models to obtain the best results for circuit designers.

Acknowledgments

The authors would like to thank former University of South Florida student Sivalingam Somasundaram Meena (now with RFMD in North Carolina) for his assistance with some of the measurements and test setups used in this work as part of a grant provided by Modelithics, Inc. to the University of South Florida. We are also grateful to the reviewers of *IEEE Microwave Magazine*, whose many editing suggestions were very helpful in improving our original draft.

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